UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/516,082	03/01/2000	Satoshi Murakami	SEL163	3545

7590 08/05/2005

Cook Alex Mcfarron Manzo
Cummings & Mehler LTD
200 West Adams ST
Suite 2850
Chicago, IL 60606

EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/516,082	MURAKAMI ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *46-49,52,53,56-79,81 and 83-138* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *46-49,52,53,56-79,81 and 83-138* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/5/05 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 46, 47, 59, 65, 89, 90, 96, 99, 100, 106, 109, 110, and 116 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. 5,818,550 in view of Yanai 6,137,552. Kadota discloses (see, for example, FIG. 1) a semiconductor device comprising a first thin film transistor formed over a TFT substrate (insulating surface) 0 wherein the first thin film transistor comprises a semiconductor film 2, source and drain region S/D, channel forming region, gate insulating film, gate electrode 3; first inter-layer insulating film (interlayer insulating film) 4, electrodes (conductive layer) 7, and pixel electrode 1. Kadota does not disclose a color filter, wherein the color filter covers the entire first thin film transistor. However, Yanai discloses (see, for example, FIG. 2) a semiconductor device comprising a color-filter layer (color filter) 8,

which covers a thin film transistor. The color-filter layer comprises red, blue, green layers in the same manner as the applicant's invention (see, for example, paragraph [0386]). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a color filter, wherein the color filter covers the entire first thin film transistor in order to provide multiple colors from a thin film transistor.

Regarding the limitation "a semiconductor film comprising crystalline silicon", see, for example, column 3, line 64 wherein Kadota discloses the semiconductor film being a polycrystalline silicon thin film.

4. Claims 48, 49, 52, 53, 60, 61, 66, 67, 91, 92, 97, 98, 101, 102, 107, 108, 111, 112, 117, and 118 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Yanai '552 as applied to claims 46, 47, 59, 65, 89, 90, 96, 99, 100, 106, 109, 110, and 116 above, and further in view of Seo 6,323,521. Kadota in view of Yanai does not disclose the interlayer insulating film comprising at least a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide. However, Seo discloses (see, for example, FIG. 6D) a semiconductor device comprising a gate insulating interlayer (interlayer insulating film) 219 over a thin film transistor. In column 9, lines 3-8, Seo discloses the gate insulating interlayer as being silicon oxide, silicon nitride or other suitable material. The gate insulating interlayer covers the thin film transistor and provides an adequate material for making contact holes. The contact holes are used to form contacts to source and drain regions of a thin film transistor. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use a material selected from the group consisting of silicon nitride, silicon

oxide and nitrated silicon oxide for the interlayer insulating film in order to cover the thin film transistor and provides an adequate material for making contact holes, and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claim 52, and 53, Kadota in view of Yanai discloses (see, for example, FIG. 1 of Kadota) a semiconductor device comprising a thin film transistor formed over a TFT substrate (insulating surface) 0 wherein the thin film transistor comprises a semiconductor film 2, source and drain region S/D, channel forming region, gate insulating film, gate electrode 3; first inter-layer insulating film (first interlayer insulating film) 4, electrodes (conductive layer) 7, second inter-layer insulating film (passivation film) 5, color filter 9R/9G/9B, and pixel electrode 1. Kadota in view of Yanai does not disclose the second inter-layer insulating film (passivation film) comprising at least a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide. However, Seo discloses (see, for example, FIG. 6D) a semiconductor device comprising a passivation film (second interlayer insulating film) 231 over a thin film transistor. In column 10, lines 2-5, Seo discloses the passivation film as being silicon oxide or silicon nitride. The passivation film covers the source and drain electrodes of the thin film transistor and provides an adequate material for making contact holes. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide in order to cover the source and drain electrodes of the thin film transistor and provide an adequate material for making contact holes, and since it has been held to be within the general skill of a

worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

5. Claims 56, 62, 71, 74, 93, 103, and 113 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Yanai '552 as applied to claims 46, 47, 59, 65, 89, 90, 96, 99, 100, 106, 109, 110, and 116 above, and further in view of Ha 5,677,207. Kadota in view of Yanai does not disclose LDD regions. However, Ha discloses (see, for example, FIG. 3G) a semiconductor device comprising LDD regions 38 in contact with a channel area 32a. In column 1, lines 48-63, Ha discloses that LDD areas reduce the electric field between the drain and channel area. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include the LDD regions in order to reduce the electric field between the drain and channel area, and reduce leakage current.

6. Claims 57, 58, 63, 64, 72, 73, 75, 76, 94, 95, 104, 105, 114, and 115 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Yanai '552 in view of Seo '521 as applied to claims 48, 49, 52, 53, 60, 61, 66, 67, 91, 92, 97, 98, 101, 102, 107, 108, 111, 112, 117, and 118 above, and further in view of Ha 5,677,207. Kadota in view of Yanai in view of Seo does not disclose LDD regions. However, Ha discloses (see, for example, FIG. 3G) a semiconductor device comprising LDD regions 38 in contact with a channel area 32a. In column 1, lines 48-63, Ha discloses that LDD areas reduce the electric field between the drain and channel area. Therefore it would have been obvious to one of ordinary skill in the art at the time

of invention to include the LDD regions in order to reduce the electric field between the drain and channel area, and reduce leakage current.

7. Claims 77, 78, and 86 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Yanai '552 as applied to claims 46, 47, 59, 65, 89, 90, 96, 99, 100, 106, 109, 110, and 116 above, and further in view of Matsumoto 5,323,042. Kadota in view of Yanai does not disclose a driver circuit comprising a second thin film transistor, wherein the pixel matrix circuit and the driver circuit are over a same substrate. However, Matsumoto discloses (see, for example, FIG. 1) a semiconductor device comprising a thin film transistor 12 for a matrix circuit and thin film transistor for a peripheral driving circuit (driver circuit) 13. In column 1, lines 8-48, Matsumoto states that an active matrix type liquid crystal display comprises a matrix circuit for applying an electric field and a peripheral driving circuit for driving the matrix circuit. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include a driver circuit in order to drive the matrix circuit.

8. Claims 79, 81, 87, and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Yanai '552 in view of Seo '521 as applied to claims 48, 49, 52, 53, 60, 61, 66, 67, 91, 92, 97, 98, 101, 102, 107, 108, 111, 112, 117, and 118 above, and further in view of Matsumoto 5,323,042. Kadota in view of Yanai in view of Seo does not disclose a driver circuit comprising a second thin film transistor, wherein the pixel matrix circuit and the driver circuit are over a same substrate. However, Matsumoto discloses (see, for example, FIG. 1) a semiconductor device comprising a thin film transistor 12 for a matrix circuit and thin film

transistor for a peripheral driving circuit (driver circuit) 13. In column 1, lines 8-48, Matsumoto states that an active matrix type liquid crystal display comprises a matrix circuit for applying an electric field and a peripheral driving circuit for driving the matrix circuit. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include a driver circuit in order to drive the matrix circuit.

9. Claim 68 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Yanai '552 as applied to claims 46, 47, 59, 65, 89, 90, 96, 99, 100, 106, 109, 110, and 116 above, and further in view of Mikoshiba 5,499,123. Kadota in view of Yanai discloses (see FIG. 1) a planarization film (resin film) 10. In column 5, lines 60-65, Kadota discloses the planarization film comprising an acrylic resin or polyimide resin used as an organic transparent material. Kadota in view of Yanai does not disclose an electrode over the organic resin film; and an oxide film of the electrode in direct contact with at least a portion of a surface of the electrode, wherein the pixel electrode is in direct contact with at least a portion of the oxide film, and wherein a storage capacitor comprises the electrode and the pixel electrode with the oxide film interposed therebetween. However, Mikoshiba discloses (see, for example, FIG. 3B) a semiconductor device comprising a capacitance element 400 wherein the capacitance element comprises a shading layer (electrode) 312, insulating layer (oxide film) 314, and transparent layer (pixel electrode) 308. In column 4, lines 57-64, Mikoshiba discloses that a bias voltages can be applied to the capacitance element so that a brighter, clearer image can be attained. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include an electrode over the organic resin film; and an oxide film of the electrode in direct

contact with at least a portion of a surface of the electrode, wherein the pixel electrode is in direct contact with at least a portion of the oxide film, and wherein a storage capacitor comprises the electrode and the pixel electrode with oxide film interposed therebetween in order to apply a bias voltage to an LCD device so that a brighter, clearer image may be attained.

10. Claims 69 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Yanai '552 in view of Seo '521 as applied to claims 48, 49, 52, 53, 60, 61, 66, 67, 91, 92, 97, 98, 101, 102, 107, 108, 111, 112, 117, and 118 above, and further in view of Mikoshiba 5,499,123. Kadota in view of Yanai in view of Seo discloses a planarization film (resin film) 10. In column 5, lines 60-65, Kadota discloses (see FIG. 1) the planarization film comprising an acrylic resin or polyimide resin used as an organic transparent material. Kadota in view of Yanai in view of Seo does not disclose an electrode over the organic resin film; and an oxide film of the electrode in direct contact with at least a portion of a surface of the electrode, wherein the pixel electrode is in direct contact with at least a portion of the oxide film, and wherein a storage capacitor comprises the electrode and the pixel electrode with the oxide film interposed therebetween. However, Mikoshiba discloses (see, for example, FIG. 3B) a semiconductor device comprising a capacitance element 400 wherein the capacitance element comprises a shading layer (electrode) 312, insulating layer (oxide film) 314, and transparent layer (pixel electrode) 308. In column 4, lines 57-64, Mikoshiba discloses that a bias voltage can be applied to the capacitance element so that a brighter, clearer image can be attained. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include the electrode over the organic resin film; and an oxide film of the electrode in direct contact with

at least a portion of a surface of the electrode, wherein the pixel electrode is in direct contact with at least a portion of the oxide film, and wherein a storage capacitor comprises the electrode and the pixel electrode with oxide film interposed therebetween in order to apply a bias voltage to an LCD device so that a brighter, clearer image may be attained.

11. Claim 83 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Yanai '552 in view of Ha '207 as applied to claims 56, 62, 71, 74, 93, 103, and 113 above, and further in view of Matsumoto 5,323,042. Kadota in view of Yanai in view of Ha does not disclose a driver circuit comprising a second thin film transistor, wherein the pixel matrix circuit and the driver circuit are over a same substrate. However, Matsumoto discloses (see, for example, FIG. 1) a semiconductor device comprising a thin film transistor 12 for a matrix circuit and thin film transistor for a peripheral driving circuit (driver circuit) 13. In column 1, lines 8-48, Matsumoto states that an active matrix type liquid crystal display comprises a matrix circuit for applying an electric field and a peripheral driving circuit for driving the matrix circuit. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include a driver circuit in order to drive the matrix circuit.

12. Claims 84 and 85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Yanai '552 in view of Seo '521 in view of Ha '207 as applied to claims 57, 58, 63, 64, 72, 73, 75, 76, 94, 95, 104, 105, 114, and 115 above, and further in view of Matsumoto 5,323,042. Kadota in view of Yanai in view of Seo in view of Ha does not disclose a driver circuit comprising a second thin film transistor, wherein the pixel matrix circuit and the

driver circuit are over a same substrate. However, Matsumoto discloses (see, for example, FIG. 1) a semiconductor device comprising a thin film transistor 12 for a matrix circuit and thin film transistor for a peripheral driving circuit (driver circuit) 13. In column 1, lines 8-48, Matsumoto states that an active matrix type liquid crystal display comprises a matrix circuit for applying an electric field and a peripheral driving circuit for driving the matrix circuit. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include a driver circuit in order to drive the matrix circuit.

13. Claims 119, 120, and 126 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Yanai '552 as applied to claims 46, 47, 59, 65, 89, 90, 96, 99, 100, 106, 109, 110, and 116 above, and further in view of Kunii et al. 5,412,493. Kadota in view of Yanai does not disclose one or more gate electrodes in addition to the gate electrode. However, Kunii discloses (see, for example, FIG. 1) a thin film transistor comprising a multi-gate structure wherein the multi-gate structure comprises two gate electrodes (one or more gate electrodes) 9. In column 7, line 67-column 8, line 11, Kunii discloses the multi-gate structure improves dispersion in gate capacitance coupling, and reduces brightness line defect. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have one or more gate electrodes in addition to the gate electrode in order to improve dispersion in gate capacitance coupling, and reduce brightness line defect.

14. Claims 121, 122, 127, and 128 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Yanai '552 in view of Seo '521 as applied to claims 48, 49,

52, 53, 60, 61, 66, 67, 91, 92, 97, 98, 101, 102, 107, 108, 111, 112, 117, and 118 above, and further in view of Kunii et al. 5,412,493. Kadota in view of Yanai in view of Seo does not disclose one or more gate electrodes in addition to the gate electrode. However, Kunii discloses (see, for example, FIG. 1) a thin film transistor comprising a multi-gate structure wherein the multi-gate structure comprises two gate electrodes (one or more gate electrodes) 9. In column 7, line 67-column 8, line 11, Kunii discloses the multi-gate structure improves dispersion in gate capacitance coupling, and reduces brightness line defect. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have one or more gate electrodes in addition to the gate electrode in order to improve dispersion in gate capacitance coupling, and reduce brightness line defect.

15. Claim 123 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Yanai '552 in view of Ha '207 as applied to claims 56, 62, 71, 74, 93, 103, and 113 above, and further in view of Kunii et al. 5,412,493. Kadota in view of Yanai in view of Ha does not disclose one or more gate electrodes in addition to the gate electrode. However, Kunii discloses (see, for example, FIG. 1) a thin film transistor comprising a multi-gate structure wherein the multi-gate structure comprises two gate electrodes (one or more gate electrodes) 9. In column 7, line 67-column 8, line 11, Kunii discloses the multi-gate structure improves dispersion in gate capacitance coupling, and reduces brightness line defect. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have one or more gate electrodes in addition to the gate electrode in order to improve dispersion in gate capacitance coupling, and reduce brightness line defect.

16. Claims 124, and 125 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Yanai '552 in view of Seo '521 in view of Ha '207 as applied to claims 57, 58, 63, 64, 72, 73, 75, 76, 94, 95, 104, 105, 114, and 115 above, and further in view of Kunii et al. 5,412,493. Kadota in view of Yanai in view of Seo in view of Ha does not disclose one or more gate electrodes in addition to the gate electrode. However, Kunii discloses (see, for example, FIG. 1) a thin film transistor comprising a multi-gate structure wherein the multi-gate structure comprises two gate electrodes (one or more gate electrodes) 9. In column 7, line 67-column 8, line 11, Kunii discloses the multi-gate structure improves dispersion in gate capacitance coupling, and reduces brightness line defect. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have one or more gate electrodes in addition to the gate electrode in order to improve dispersion in gate capacitance coupling, and reduce brightness line defect.

17. Claim 129, 130, and 136 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Yanai '552 as applied to claims 46, 47, 59, 65, 89, 90, 96, 99, 100, 106, 109, 110, and 116 above, and further in view of Kadota et al. 6,031,512. Kadota '550 in view of Yanai '552 does not disclose the gate electrode being covered by the interlayer insulating film. However, Kadota '512 discloses (see, for example, FIG. 1) a gate electrode covered by an interlayer insulating film 4. The interlayer insulating film provides additional protection to the gate electrode. Therefore, it would have been obvious to one of ordinary skill

in the art at the time of invention to have the gate electrode being covered by the interlayer insulating film in order to provide additional protection to the gate electrode.

18. Claim 131, 132, 137, and 138 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Yanai '552 in view of Seo '521 as applied to claims 48, 49, 52, 53, 60, 61, 66, 67, 91, 92, 97, 98, 101, 102, 107, 108, 111, 112, 117, and 118 above, and further in view of Kadota et al. 6,031,512. Kadota '550 in view of Yanai in view of Seo does not disclose the gate electrode being covered by the interlayer insulating film. However, Kadota '512 discloses (see, for example, FIG. 1) a gate electrode covered by an interlayer insulating film 4. The interlayer insulating film provides additional protection to the gate electrode. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the gate electrode being covered by the interlayer insulating film in order to provide additional protection to the gate electrode.

19. Claim 133 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Yanai '552 in view of Ha '207 as applied to claims 56, 62, 71, 74, 93, 103, 113, and 123 above, and further in view of Kadota et al. 6,031,512. Kadota '550 in view of Yanai in view of Ha does not disclose the gate electrode being covered by the interlayer insulating film. However, Kadota '512 discloses (see, for example, FIG. 1) a gate electrode covered by an interlayer insulating film 4. The interlayer insulating film provides additional protection to the gate electrode. Therefore, it would have been obvious to one of ordinary skill in the art at the

time of invention to have the gate electrode being covered by the interlayer insulating film in order to provide additional protection to the gate electrode.

20. Claim 134, and 135 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Yanai '552 in view of Seo '521 in view of Ha '207 as applied to claims 57, 58, 63, 64, 72, 73, 75, 76, 94, 95, 104, 105, 114, and 115 above, and further in view of Kadota et al. 6,031,512. Kadota '550 in view of Yanai in view of Seo in view of Ha does not disclose the gate electrode being covered by the interlayer insulating film. However, Kadota '512 discloses (see, for example, FIG. 1) a gate electrode covered by an interlayer insulating film 4. The interlayer insulating film provides additional protection to the gate electrode. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the gate electrode being covered by the interlayer insulating film in order to provide additional protection to the gate electrode.

Response to Arguments

21. Applicant's arguments with respect to claims 46-49, 52, 53, 56-79, 81, and 83-138 have been considered but are moot in view of the new ground(s) of rejection.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
July 23, 2005